

Reducing Hardware Requirements and Error for Hybrid Computing System

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Abstract: *Computing techniques are widely used in all areas and there is no area of human activity, where could not find devices which are built on electronic computing systems. Performance of computing system can be determined by calculation with minimum error, minimum hardware requirements and minimum computing time. In any computing systems, their performance depended on three basic characteristics: speed, accuracy and hardware requirements. Improvement of any of these three characteristics is the important task in Science and Technology Engineering. This paper presents reducing hardware requirements and error for hybrid computing systems based on double precision method. The traditional computing system has many computing errors. . In some cases, accuracy of computing system is still required. For example, controlling the weapon in military services is very important. To get accurate control for necessary target, it is needed to develop the accuracy by reducing error. Hybrid computing system is suitable for increasing computing accuracy because it accepts both analog and digital forms. This paper intends to reduce the minimum hardware requirement in symmetric and asymmetric division for arithmetic operations with double precision method and also uses security bits to detect error. This paper is also verified with programming package MATLAB for hardware reducing portion and error reducing portion.*

Keywords: *accuracy, computing systems, double precision method, hardware requirement.*

1. Introduction

Today, input and output information of real time automatic control systems are represented in a mixed form of analog and digital. There is well known analog-digital computing system in which basics arithmetic operations are realized used as a special computing unit [1]. Moreover, their application areas have practically captured in all sphere of human activity. Depending on representation and processing of information, computing system can be classified into three: Analog Computing System (ACS), Digital computing System (DCS) and Analog-Digital Computing System (ADCS) or Hybrid Computing System (HCS). If input data is the combination of digital and analog, using ACS and DCS takes longer computing time than using the converting time for relevant system. Hybrid computing system (HCS) uses ADC, DAC as computing units so no more converting is needed and processing time is minimum but it may have error when computing arithmetic operation [2]. To reduce this error, this paper proposes double precision method used in digital computing system. Although there was no problems in DCS by using double precision method, HCS has error because it accumulates them when computing arithmetic operation. There are many applications with the usage of hybrid computing system. Hybrid systems have been used as mathematical models for many important applications, such as automated highway systems, air-traffic management systems, embedded automotive controllers, manufacturing systems, chemical processes, robotics, real-time communication networks, space-rocket technologies, missile path control and real-time circuits [3]. In some cases, accuracy of computing system is still required. For example, controlling the weapon in military services is very important. To get accurate control for necessary target, it is needed to develop the accuracy and processing time. Performance of computing system can be determined by calculation with minimum error, minimum hardware requirements and minimum computing time. Fig.1 shows characteristics of computing system. In any computing systems their performance depended on three basic characteristics. They are speed, accuracy and hardware requirements.

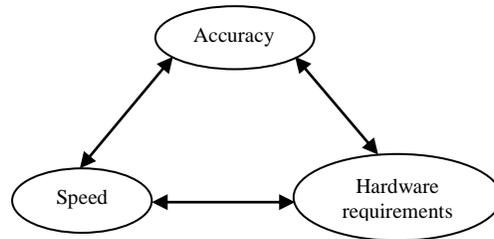


Fig. 1: Characteristics of computing system.

2. Related Work

This algorithm is based on double precision method used in digital computing system. To reduce the error, developed double precision method for HCS was proposed [4]. Using double precision method can calculate input operands with $2n$ bits length in n bits computing machine and it is appropriate to solve the problems with fixed point numbers. For implementation of this method, it needs to divide input operands in two parts (or more) and needs to multiply these parts (for multiplication operation) [5]. Double precision method for HCS includes the following steps.

- Calculating arithmetic operation without dividing input operands for getting one answer
- Dividing input operands into two parts: most significant bits (MSB) and least significant bits (LSB)
- Calculating one result by adding intermediate products (to get the sum of partial product)
- Error can be reduced by using control bits of two results (full product and sum of partial product)

The result of calculation by a principle of division operands in conditions of an error with complete product (full product) and sum of partial products (sum of product) can be formed. The control bits can be any bits (1-12 bits). Thus, most senior bits among these bits are nominated as control, as they are by smaller errors. Therefore, bits (8, 9 and 10) in complete product and sums of partial products are named as the control bits. By using three control bits, the system gets at least 10^{th} bit accuracy and at most 13^{th} bit accuracy in 24 bit [6]. Multiplication operation with double precision method and error correction with control bits (8,9,10) is shown in Fig 2. The operation time formula for this method can be calculated in the following equation.

$$\text{System operation time, } T_j = T_f + 40 T_c + 4(T_1 + T_2)$$

where, T_f -time for full product

T_1 -time of multiplication for partial product

T_2 -time of addition for partial product

T_c - control bit checking and comparison time

T_j - result formation time

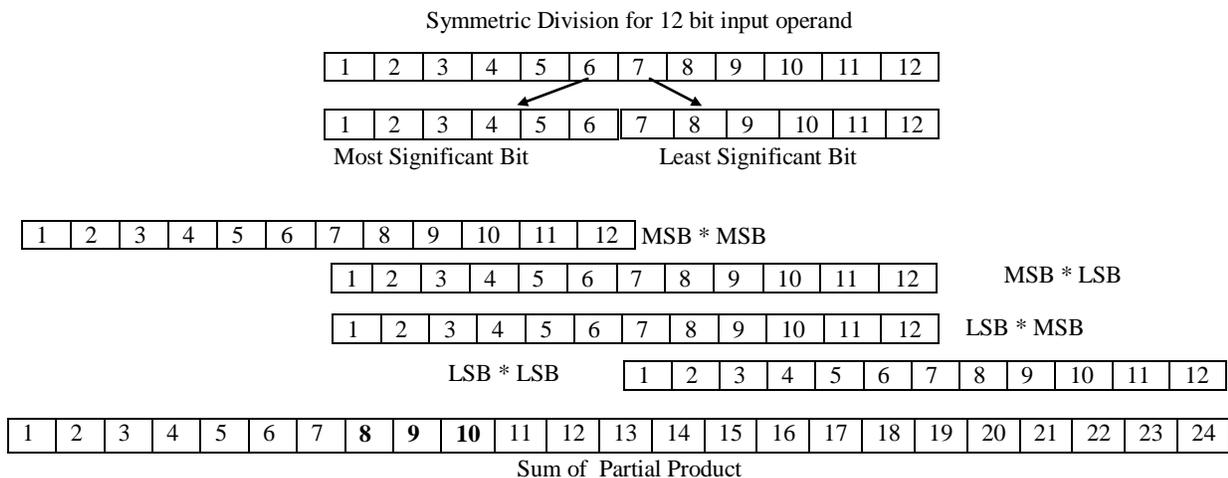


Fig. 2: Multiplication with double precision method and error correction with control bits (8,9,10)

3. Research Method

Performance of computing system can be determined by calculation of given operation with minimum errors, minimum computing time and minimum hardware requirements. In my paper, there are two portions: hardware reducing portion and error reducing portion.

3.1. Hardware Reducing of Proposed System

The minimum hardware requirement is important. To compare hardware requirement in multiplication operation, we consider 12 bits input operands. Proposed algorithms for symmetric and asymmetric division are shown in Fig. 3 and 4.

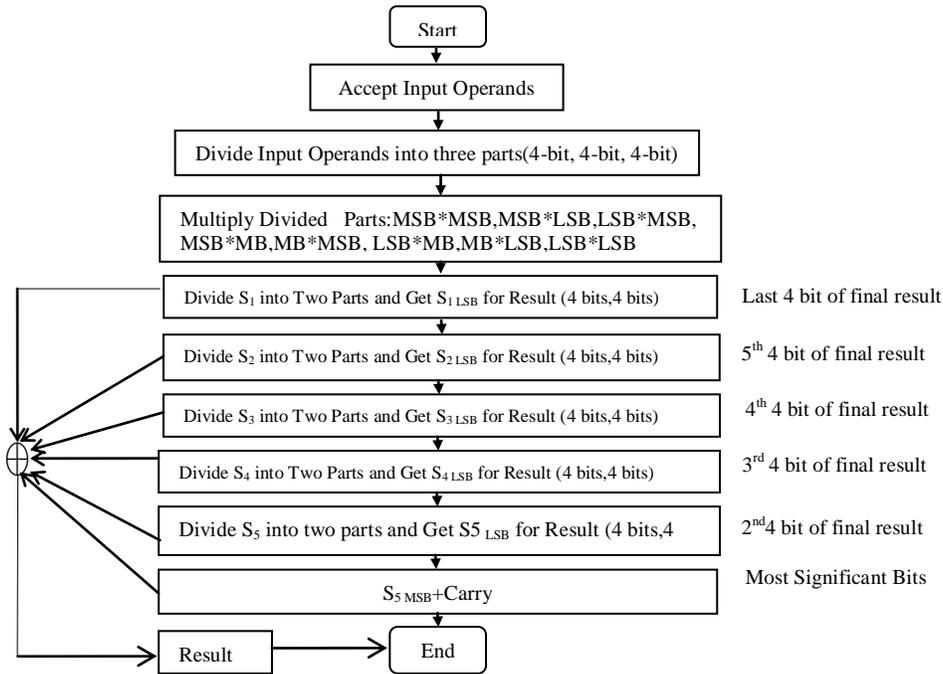


Fig. 3: Flowchart of symmetric division algorithm

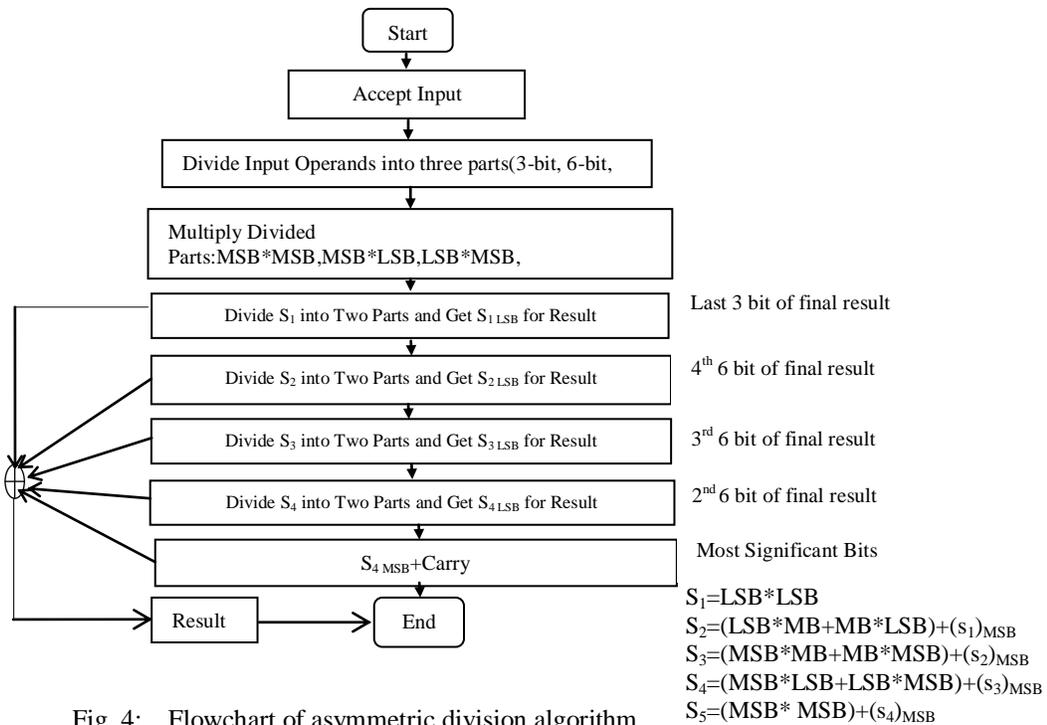


Fig. 4: Flowchart of asymmetric division algorithm

In this paper, for symmetric division, we divide $a_{MSB}=6$, $b_{MSB}=6$ bits and $a_{LSB}=b_{LSB}=6$ bits (MSB=LSB). Symmetric division algorithm for my proposed system is shown in Figure 3. In asymmetric division (MSB<LSB), $a_{MSB} = b_{MSB} = 3$ bits and $a_{LSB} = b_{LSB} = 9$ bits and (MSB>LSB), $a_{MSB} = b_{MSB} = 9$ bits and $a_{LSB} = b_{LSB} = 3$ bits. If the number of most significant bits (m) are equal to the number of least significant bits (l), the number of two input AND gates are $(m \cdot l)$, the number of half-adder is m and the number of full-adder is $m \cdot (l-2) = 6 \cdot (6-2) = 24$. Asymmetric division algorithm for my proposed system is shown in Figure 4. If the number of most significant bits (m) is not equal to the number of least significant bits (l), in other words, if the number of most significant bits (m) is less than or greater than the number of least significant bits (l), the number of two input AND gates is $(m \cdot l)$, the number of half-adder is m and the number of full-adder is $(m+1+2)$.

As one half-adder has XOR gate and one AND gate, and one full-adder has two XOR gates, two AND gates and one OR gate. The comparison of hardware requirements before and after using double precision method for symmetric and asymmetric division is shown in Table 1. So, the hardware requirements in asymmetric division are less than the hardware requirements in symmetric division after using the double precision method. It can reduce 384 gates for symmetric division and 934 gates for asymmetric division in total gates.

TABLE I: Results for before and after double precision method

Hardware Requirements Before using Double Precision Method								
Symmetric(MSB = LSB)			Asymmetric(MSB < LSB)			Asymmetric(MSB > LSB)		
AND gate	OR gate	NOT gate	AND gate	OR gate	NOT gate	AND gate	OR gate	NOT gate
834	332	460	845	338	446	845	338	446
Hardware Requirements After using Double Precision Method								
Symmetric(MSB = LSB)			Asymmetric(MSB < LSB)			Asymmetric(MSB > LSB)		
AND gate	OR gate	NOT gate	AND gate	OR gate	NOT gate	AND gate	OR gate	NOT gate
636	254	352	809	326	448	359	140	196

3.2. Error Reducing of Proposed System

Hybrid computing system use double precision method to reduce errors in digital computing system. It is appropriate to solve the problems with fixed point numbers and it is able to realize arithmetic operations with $2n$ bit input operands on n bit computing system. The calculation with double precision method is considered on an example of flow diagram of multiplication operation for two operands a and b. Furthermore, implementation of this method, it needs to divide input operands in two parts (or more) and needs to multiply these parts (for multiplication operation). Double precision method for HCS includes the following steps:

- Dividing input operand into two parts: Most Significant Bit (MSB) and Least Significant Bit (LSB)
- Error can reduce by assigning security bits the value 0 and 1 at bit 13th and 14th position.

In the system, input operand is divided into three parts: Most Significant Bit (MSB) and Least Significant Bit (LSB). Multiplication is needed to compute intermediate result. This result can get by multiplication of divided parts and sum intermediate results. In this system, we use security bits to detect and correct error instead of control bit. The value of security bits are between 00 and 11. In this paper, the value 01 is assign default value for security bit. After finishing multiplication operation, the values 0 and 1 assigns bit 13th and 14th position as security bits. The next stage needs to add the result of multiplication parts. In this stage, the system needs to check error in bit position 13th and 14th position. If security bits are 00 and 10, the system needs to add the value 01 to security bits and to subtract the value 01 from security bits. . If security bits are 11, the system needs to subtract the value 10 from security bits. . If security bits are 10, no operations needed for security bits. After checking the summation process, the system also needs to check error at bit 8th position. If error shows bit 12th, it needs to check error at bit 8th to get original value. After checking this stage, the system extracts and gets final result. Fig. 5 and 6 show the multiplication with symmetric division with security bit for error checking. The operation time formula for this method can be calculated in the following equation.

System operation time, $T_j=4(T_1+T_2)$

Where, T_1 -time of multiplication for partial product

T_2 -time of addition for partial product

T_j - result formation time

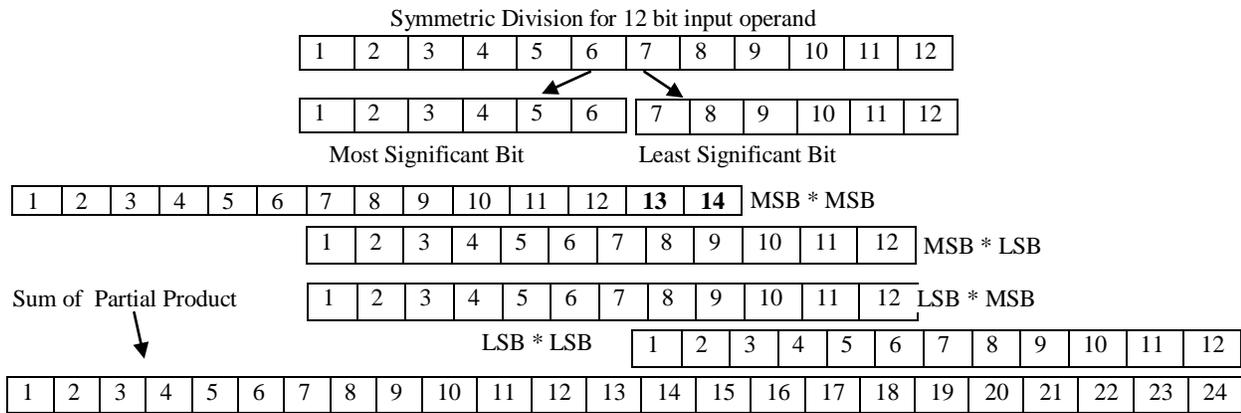


Fig. 5: Multiplication with symmetric division with security bit for error checking

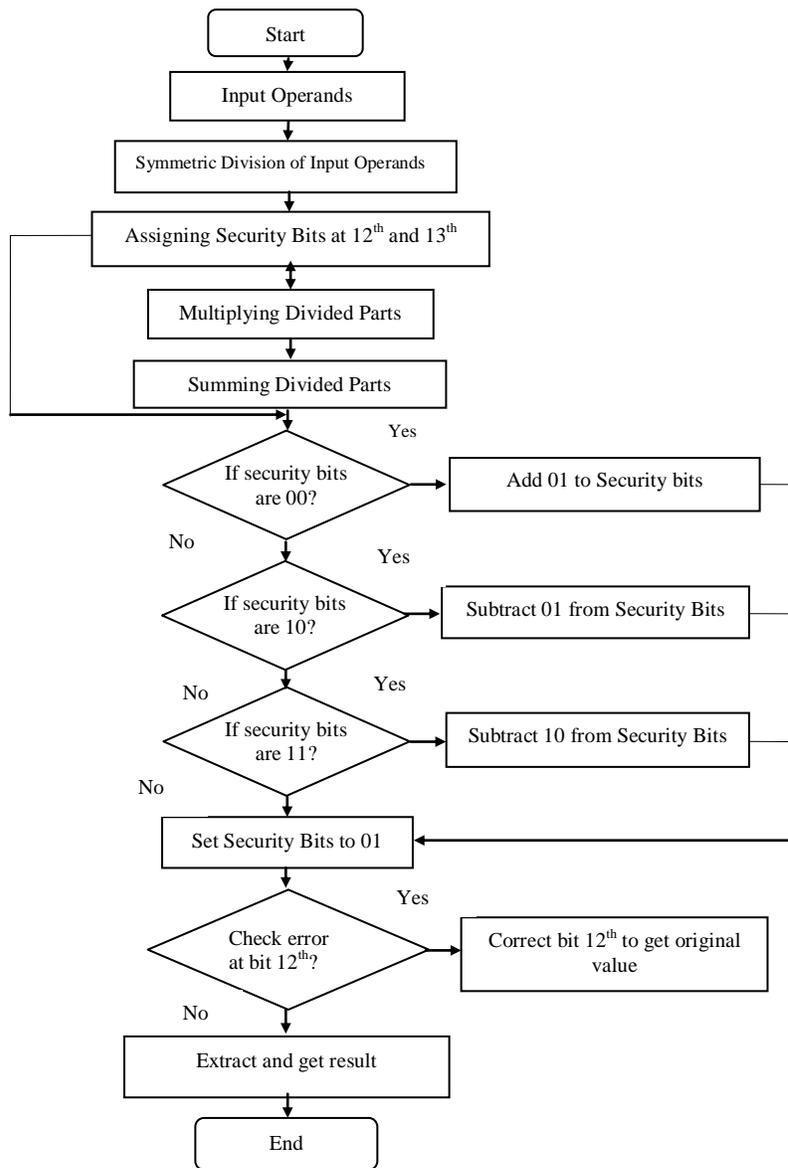


Fig. 6: Flowchart of proposed system

4. Verification Results

In my proposed system, there are four portions in hardware reduce for symmetric division algorithm. The number of AND gate is 900 gates in two division. In five division, the number of AND gate is approximately over 300 gates. Fig. 7 and 8 show hardware reduce for symmetric and asymmetric division algorithm using double precision method.

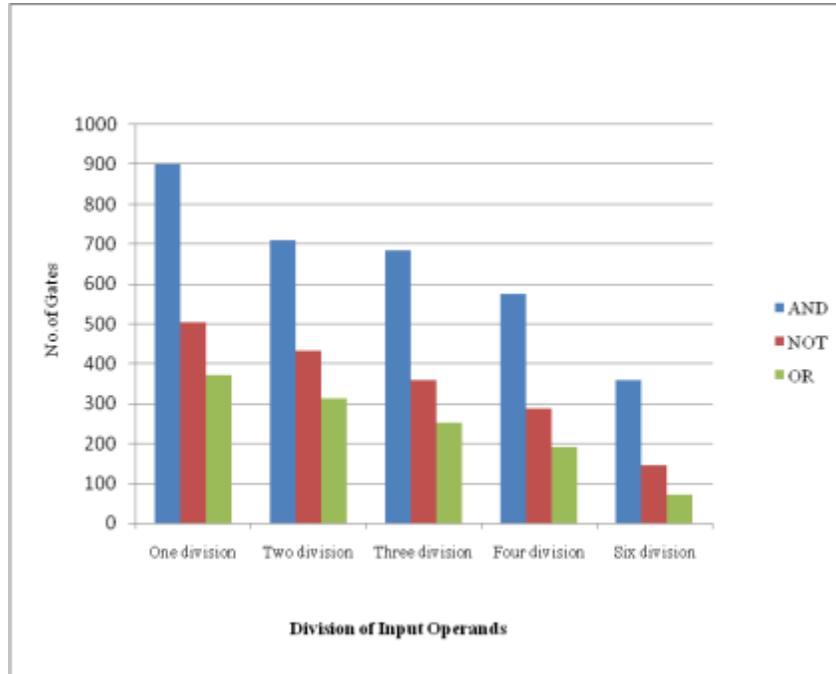


Fig. 7: Hardware reduce for symmetric division

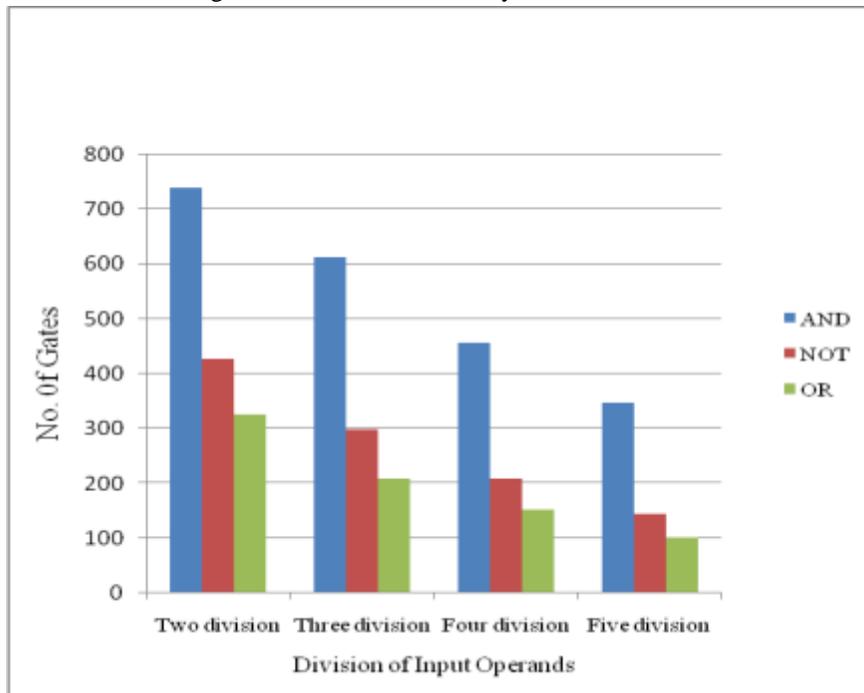


Fig. 8: Hardware reduce for asymmetric division

Fig. 9 shows the comparison of operation time using control bits and security bits. During error reduction process, the operation time using security bit is less than control bit.

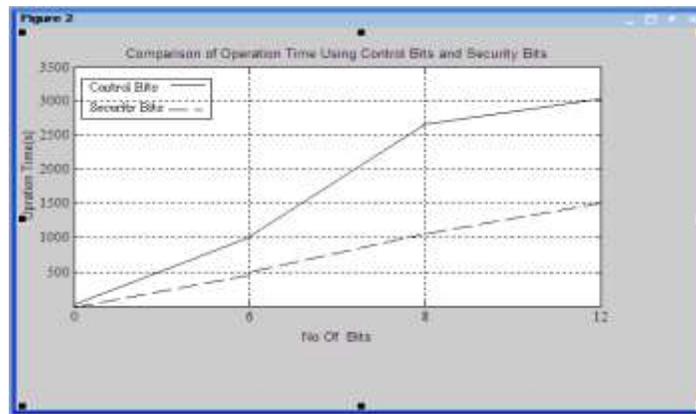


Fig. 9: Comparison of operation time using control bits and security bits

5. Conclusions

The calculation technique is developed on a method of division of operands for the analogue-digital computing structures that is allowed to increase accuracy of calculations. The correction technique of computing results in analyzing of security bits is also developed. Symmetric division allows raising accuracy in result of 24 equivalent bits compare with other method. The increasing quantity of using security bit is twice than of control bit in accuracy. During error reduction process, the operation time for this system is less than the other method because this method does not need the time for full product. The hardware requirements in asymmetric division are less than the hardware requirements in symmetric division after using the double precision method. According to my research, the more we divide the hardware, the more we reduce. In the future work, computing technique by operand division will verify with the example of symmetric and correction by result restoration with the help of MATLAB programming language.

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7. References

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